AMENDMENT TO THE CLAIMS

1-2. (Canceled)

3. (Currently amended) ~~The integrated circuit of claim 1~~ An integrated circuit having a multiprocessor architecture, the circuit comprising:

a first processor, which operates synchronously with a first internal clock signal;

a second processor, which operates synchronously with a second internal clock signal;

a memory, which operates synchronously with a third internal clock signal; and

a clock supply unit, which respectively adjusts the delays of three clock signals generated from an external clock signal and respectively supplies the three clock signals as the first, the second and the third internal clock signals, such that the first, the second and the third internal clock signals are in phase with each other;

wherein the first processor, the second processor, the memory, and the clock supply unit are integrated together on a single chip,

wherein the clock supply unit further,

receives a first terminating signal and a second terminating signal;

stops supplying all of the first, second and third internal clock signals when the first and second terminating signals are asserted at the same time;

stops supplying only the first internal clock signal when the first terminating signal is solely asserted; and

stops supplying only the second internal clock signal when the second terminating signal is solely asserted.

4. (Canceled)

5. (Currently amended) ~~The integrated circuit of claim 4~~ An integrated circuit having a multiprocessor architecture, the circuit comprising:

a first processor, which operates synchronously with a first internal clock signal;

a second processor, which operates synchronously with a second internal clock signal;

a memory, which operates synchronously with a third internal clock signal; and

a clock supply unit, which respectively adjusts the delays of three clock signals generated from an external clock signal and respectively supplies the three clock signals as the first, the second and the third internal clock signals, such that the first, the second and the third internal clock signals are in phase with each other;

wherein the first processor, the second processor, the memory, and the clock supply unit are integrated together on a single chip,

wherein the integrated circuit further comprises a reset control unit that is integrated on the chip, the reset control unit supplying a first internal reset signal, a second internal reset signal and a third internal reset signal, the first internal reset signal being used for resetting the memory, the second internal reset signal being used for resetting the first processor, the third internal reset signal being used for resetting the second processor,

wherein the reset control unit,

receives a first external reset signal, a second external reset signal, and a third external reset signal;

asserts all of the first, second and third internal reset signals when the first external reset signal is asserted;

asserts only the second internal reset signal when the second external reset signal is asserted; and

asserts only the third internal reset signal when the third external reset signal is asserted,

wherein the clock supply unit further,

receives a first terminating signal and a second terminating signal;

stops supplying all of the first, second and third internal clock signals when the first and second terminating signals are asserted at the same time;

stops supplying only the first internal clock signal when the first terminating signal is solely asserted; and

stops supplying only the second internal clock signal when the second terminating signal is solely asserted.

6. (Previously presented) An integrated circuit having a multiprocessor architecture, the circuit comprising:

a first processor, which operates synchronously with a first internal clock signal;

a second processor, which operates synchronously with a second internal clock signal;

a memory, which operates synchronously with a third internal clock signal; and

a clock supply unit, which respectively supplies three clock signals generated from an external clock signal as the first, the second and the third internal clock signals, wherein

the first processor, the second processor, the memory, and the clock supply unit are integrated together on a single chip, and

the clock supply unit,

receives a first terminating signal and a second terminating signal;

stops supplying all of the first, second and third internal clock signals when the first and second terminating signals are asserted at the same time;

stops supplying only the first internal clock signal of the first, second and third internal clock signals when only the first terminating signal of the first and second terminating signals is asserted; and

stops supplying only the second internal clock signal of the first, second and third internal clock signals when only the second terminating signal of the first and second terminating signals is asserted.

7. (Canceled)